COCK PULSE MULTIPLIER

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Inventor(s): MIURA KIYOSHI
Applicant(s):: SONY CORP
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Abstract

PROBLEM TO BE SOLVED: To provide a cock pulse multiplier capable of generating a clock pulse with highly accurate repeat frequency without jitter with simplified structure.
SOLUTION: Four phase clocks with mutual phase difference of 90 deg. are outputted from a clock generation circuit 10. A first intermediate signal Fa which rises at the rise of a first clock Fk1 and falls at the rise of a second clock Fk2 is outputted from an S-R latch circuit 11 where the first clock Fk1 and the second clock Fk2 are inputted to the set terminal S and the reset terminal R, respectively. Further, a second intermediate signal Fb which rises at the rise of a third clock Fk3 and falls at the rise of a fourth clock Fk4 is outputted from an S-R latch circuit 11 to of the third clock Fk3 and the fourth clock Fk4 are inputted. The first and the second intermediate signals Fa, Fb are alternately selected by a selector 12. As a result, a clock pulse Fo with highly accurate repeat frequency is outputted from the selector 12 without being affected by the duty ratio of the four phase clock.